REMARKS

Applicant thanks Examiner for the detailed review of the application.

Claim Objections

The Office Action currently objects to applicant's claims 18-20 because of lack of antecedent basis in reference to "processor die" in line 6 of claim 18. Claim 18 has been amended to remove the reference to chip or die. Claim 18 now refers to "a processor including" and "associated with the processor." Therefore, applicant respectfully requests that the informalities of claim 18-20 have been properly corrected.

Claim Rejections -35 USC § 103(a)

The Office Action has rejected Claims under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,195,728 to Bordaz et al. (referred to hereinafter as "Bordaz") in view of US. 6,134,631 to Jennings et al. (herein referred to as "Jennings").

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has failed to meet one or more of these requirements.

Bordaz states, at col. 3 line 67 through col. 4 lines 1-2, the following:

> FIG. **1** shows an example of machine architecture with nonuniform memory access, made up of four modules **10**, **20**, **40** and **60**, which are interconnected by means of a ring **16**. The following description of FIG. **1** is valid for any

Here, it is clear that only modules 10, 20, 40, and 60 are interconnect by a ring. In direct contrast, applicant's claim 1 includes the element, "a ring to connect **the one or more processor cores and the shared cache**," (emphasis added). As can be readily seen, processor 1-4 of Bordaz do not connect to cache element 5 in a ring, but rather in a conventional multi-drop interconnect. Therefore, Bordaz only suggests coupling of modules 10, 20, 40, and 60 in a ring, and inclusion of a cache 5 in each module and a private cache in each modules individual processor; however, there is no suggestion or description of "a ring **to connect the one or more processors and the shared cache,**" as in applicant's claim 1.

Furthermore, the combination of Bordaz and Jennings is only cited to correct Bordaz' deficiency in regards to the one or more processor cores, the shared cache, and the ring being included in an integrated circuit. However, Jennings does not disclose or suggest coupling a shared cache in a ring with processor cores.

Similarly, applicant's 14 includes the element, "a plurality of cores and a shared memory connected in a ring." Furthermore, applicant's claim 18 includes the element, "a plurality of cores and a shared memory coupled together with an unbuffered bi-directional ring interconnect." As stated above, neither Bordaz or Jennings discloses coupling of a shared memory **and** a plurality of cores in a ring, or with an unbuffered bi-directional ring interconnect, on an integrated circuit, as in applicant's claims 14 and 18, respectively.

Therefore, applicant respectfully submits that claims 1-20 are in condition for allowance for at least the reasons stated above.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
Intel Corporation

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